PLEASE AMEND THE CLAIMS AS FOLLOWS:

Claim 1. (Currently amended) A method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate, comprising the steps of:

providing a semiconductor substrate of a first conductivity type;

forming a silicon on insulator (SOI) layer on said semiconductor substrate;

forming an insulator filled, shallow trench isolation (STI) region in the silicon component of the SOI layer, with depth of said STI terminating at the top surface of the insulator component of said SOI layer;

forming a gate insulator layer on surface of said silicon component of said SOI layer;

forming a conductive gate structure on said gate insulator layer, and on a portion of said STI region;

forming a body contact region entirely in a first portion of said silicon component of said SOI region; and

forming a source/drain region in a second portion of said silicon component of said SOI layer, wherein said second portion of said silicon component of said SOI layer is separated from said first portion of said silicon component of said SOI layer by said STI region.

Claim 2. (Original) The method of claim 1, wherein said semiconductor substrate of said first conductivity type, is a P type semiconductor substrate.

Claim 3. (Original) The method of claim 1, wherein said insulator component of said SOI layer is a silicon oxide layer formed at a thickness between about 1000 to 3000 Angstroms.

Claim 4. (Original) The method of claim 1, wherein said silicon component of said SOI layer is formed at a thickness between about 1000 to 3000 Angstroms.

Claim 5. (Original) The method of claim 1, wherein said STI region is formed with an area between about 2Lg x 2Lg to 10Lg x 10Lg um^2, wherein Lg is the gate length.

Claim 6. (Original) The method of claim 1, wherein depth of said STI region is between about 1000 to 3000 Angstroms.

Claim 7. (Original) The method of claim 1, wherein said STI region is filled with silicon oxide.

Claim 8. (Original) The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer, thermally grown to a thickness between about 10 to 100 Angstroms.

Claim 9. (Original) The method of claim 1, wherein said conductive gate structure is comprised of polysilicon, at a thickness between about 1000 to 2000 Angstroms.

Claim 10. (Original) The method of claim 1, wherein an NMOS device is comprised with a N type source/drain region obtained via implantation of arsenic or phosphorous ions at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 $atoms/cm^2$.

Claim 11. (Original) The method of claim 1, wherein a PMOS device is comprised with a P type source/drain region, obtained via implantation of boron or BF_2, at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2, and comprised with an N type body contact region obtained via implantation of arsenic or phosphorous, at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2.

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Claim 12. (Currently amended) A method of forming an N channel MOSFET device and a P channel MOSFET device on a silicon on insulator (SOI) layer, featuring insulator filled, shallow trench isolation (STI) regions used to reduce parasitic transistor formation underlying the junction of conductive gate structure and ~~a~~ body contact ~~region~~ regions, comprising the steps of:

forming said SOI layer on a P type semiconductor substrate, with said SOI layer comprised of an underlying silicon oxide layer, and an overlying silicon layer;

forming shallow trench shapes in said silicon layer exposing top surface of said insulator layer;

filling said shallow trench shapes with silicon oxide resulting in insulator filled, STI regions in said silicon layer, terminating at the top surface of said SOI layer;

forming a silicon dioxide gate insulator layer on said silicon layer;

forming ~~a~~ polysilicon gate ~~structure~~ structures on said silicon dioxide gate insulator layer and on portions of said STI regions, with shape of ~~said~~ a first polysilicon gate ~~structures~~ structure used for said P channel MOSFET device separating an active device region on a first portion of said silicon layer, from non-active device regions located on second portions of said silicon layer and with a shape of a second polysilicon gate structure used for said N channel MOSFET device separating an active device region on a first portion of said silicon layer, from non-active device regions located on second portions of said silicon layer;

defining a P type body contact region for said N channel MOSFET device ~~or~~ and defining an N type body contact region for a P channel MOSFET region, with body contact regions formed entirely in said second portion of said silicon layer; and

forming an N type source/drain region for said N channel MOSFET device, ~~or~~ and forming a P type source/drain region for said P channel MOSFET device in an area of said first portion of said silicon layer not covered by said polysilicon gate structure and not covered by said polysilicon gate structure for a P channel device.

Claim 13. (Original) The method of claim 12, wherein said silicon oxide layer of said SOI layer is formed at a thickness between about 1000 to 3000 Angstroms.

Claim 14. (Original) The method of claim 12, wherein said silicon layer of said SOI layer is formed at a thickness between about 1000 to 3000 Angstroms.

Claim 15. (Original) The method of claim 12, wherein said shallow trench shapes are formed via reactive ion etching procedures to a depth between about 1000 to 3000 Angstroms.

Claim 16. (Original) The method of claim 12, wherein said STI regions are formed with an area between about 2Lg x 2Lg to 10Lg x 10Lg um^2, wherein Lg is the gate length.

Claim 17. (Original) The method of claim 12, wherein said silicon dioxide gate insulator layer is thermally grown to a thickness between about 10 to 100 Angstroms.

Claim 18. (Currently amended) The method of claim 12, wherein the thickness of said polysilicon gate ~~structure~~ structures is between about 1000 to 2000 Angstroms.

Claim 19. (Currently amended) The method of claim 12, wherein said polysilicon gate ~~structure~~ structures are ~~is~~ defined as a "T" shape gate ~~structure~~ structures.

Claim 20. (Currently amended) The method of claim 12, wherein said polysilicon gate ~~structure is~~ structures are defined s an "H"shape gate structure.

Claim 21. (Currently amended) The method of claim 12, wherein P type source/drain region of said P channel MOSFET device is formed in said first portions of said silicon layer via implantation of boron or BF_2 ions at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2.

Claim 22. (Currently amended) The method of claim 12, wherein N type source/drain region of said N channel MOSFET device is formed in said first portion of said silicon layer via implantation of arsenic or phosphorous ions at an energy between about 5 to 40 KeV, at a dose between about 2E15 to 8E15 atoms/cm^2.

Claims 23 - 44 (cancelled)